Power, Noise & Reliability for Analog & Mixed Signal Designs

2016 ANSYS Convergence Conference
ANSYS Vision for Electronics Industry

Best-in-Class Physics
Unified Workflows
Multi-physics Convergence

Electromagnetic
Electrical
Power
Thermal, Fluid
Structural
Reliability
Drivers for Semiconductor IP Market

The Internet of Things (IoT) Revolution
- Shifting SoC design towards analog/IP designs
- Over 50B connected devices by 2020

Automotive Electronics
- Increasing and complex semiconductor IPs in automobiles
- Automotive electronics cost projected to be 50% by 2030

Mobile Computing
- Large scale IP integrations to expand functionality
- Growth in supporting markets such as PMIC, Memory & WLPs
Top Challenges for IP/AMS Designers

- Multiple IP validation and modeling for SoC
- Increasing Analog & Digital cross domain integration
- Tighter reliability margins from process migrations
Totem: Analog & Mixed Signal Power-Noise-Reliability

- Power Noise
  - IR/DvD
- Power/Signal
  - EM
- Substrate Noise
- ESD Analysis
- IP Model Creation

Totem™
Benefits of Totem

- Versatility
  - SRAM/DRAM/FLASH
  - Mixed Signal Designs
  - RF Designs/Image Censors
  - HSIO/DDR/SERDES

- Accuracy
  - Silicon correlated extraction
  - PG + Substrate Extraction
  - Pico-Second simulation resolution

- Capacity
  - Full-Chip hierarchical analysis
  - Simultaneous multi-domain analysis

- Integration
  - Accurate multi-state multi-vector model creation
  - SoC integration for IP enabled
Early PDN Planning

**Focus:** Early power grid and substrate noise planning

- **Early Analysis**
  - Global PDN planning
  - Bump planning
  - Substrate isolation

- **Grid Weakness Analysis**
  - Relatively weaker region in the layout
  - Short Path Trace (SPT) for debugging

- **Substrate Noise Analysis**
  - Noise w/o pkg
  - Noise w/ pkg

- **Results**
  - Grid Weakness
  - Missing vias
  - P2P Resistance Calculation
  - Static IR Analysis
  - Substrate Noise Analysis

- **Graphs**
  - Red > -30dBV
  - Noise w/o pkg
  - Noise w/ pkg
  - -20dBV inc w/ pkg
SERDES - Requirements for Power Integrity Analysis

- Early Power Delivery Network (PDN) Planning
- Detailed Noise analysis and multi-state modeling at sub block level (eg.,) Serializer/Tx/Rx block levels
- Hierarchical Full SerDes IP (w/ multiple lanes) level analysis
Case Study: SERDES Grid Weakness Check

- Grid weakness map is the normalized resistance of all transistors in the design
- Highlights weakly connected transistors
PDN Noise sign-off

Focus: Understand and Mitigate Noise coupling issues

- DvD Noise
- Substrate Noise

✓ Vectored analysis/Multi-mode analysis
✓ Line/Load Regulation Modeling of On-Die LDO
✓ Chip Power Model for System level EMI/EMC Analysis
✓ Substrate Noise Coupling Analysis

Dynamic Power Noise

LDO output Voltage
Case Study: LDO modeling and DvD Analysis

<table>
<thead>
<tr>
<th>Method</th>
<th>peak drop</th>
</tr>
</thead>
<tbody>
<tr>
<td>HSPICE</td>
<td>160 mV</td>
</tr>
<tr>
<td>Proposed</td>
<td>142 mV</td>
</tr>
<tr>
<td>Conventional</td>
<td>12 mV</td>
</tr>
</tbody>
</table>
Substrate Noise Coupling Analysis

Case study: NXP (Saturn SAF360X)

- Multi-standard software-defined radio co-processor capable of decoding all three major digital terrestrial radio standards
- 6 separate IC functions in one chip == 75% size reduction

Coupling Noise from switching digital to sensitive analog through the silicon

Device Level
Threshold voltage modulation

Circuit Level
Functionality / performance issues in Analog & RF circuits

System Level
Preventing integration of sensitive circuits

Noise Coupling Analysis for Advanced Mixed-Signal Automotive ICs @DAC 2014
EM Reliability – Key Concerns

**Electromigration and Thermal Reliability**

- **Large Switching Voltages/Currents → Self-Heating**
- **Higher Integration → Poor Heat dissipation**
- **Poor heat dissipation → Poor thermal conductivity**

Higher temperature → Poor regulation, Higher EM

\[
P = IV = \frac{V^2}{R}.\]

\[
\kappa(T) = \kappa_0 \left( \frac{T}{T_0} \right)^{\alpha_\kappa}
\]
EM Reliability Checks

Focus: Improved Electromigration coverage

Reliability
- EM
- Thermal

- Power EM
- Pad Placement Checks
- Signal EM Analysis

Power EM/Current Density
- Power EM
- Pad Cur Map
- Power EM, pad EM limits, etc.

Signal EM on Big MOSFET Drivers/Level Shifters
- Signal EM analysis
- Driver checks
- Data and clock signal EM, driver checks
Thermal Reliability Checks

Focus: Improved coverage on Thermal Reliability and Thermal Aware EM

- Thermal aware EM
- Chip Thermal Model
- Package/System level Thermal Sign-off

HiSilicon reported 13 °C Delta-T on wire of a PLL circuit on 16nm node and compared EM w/ and w/o LTE (self-heat)

Significantly more EM violations from Self-Heat

Integrated Solution that supports Thermal aware EM Analysis
IP Modeling for SoC Sign-Off

Design IP and Verify

- Totem™
- IP Data
- SoC Constraints
- ✓ IP EM/IR/DvD sign-off
- ✓ IP detailed analysis
- ✓ IP boundary condition sign-off
- ✓ Multi-state analysis

Custom Macro Models (CMM)

Validate SoC with IP

- RedHawk™
- SoC Data
- IP Models
- ✓ Full-chip EM/IR/DvD sign-off
- ✓ IP aware analysis
- ✓ IP boundary condition sign-off
- ✓ Multi-state IP models
Case Study: IP Modeling

Instance Level Voltage Drop Map

SoC instantiating the hierarchical models generated using Totem

Xtor Level Voltage Drop of Mem1 (WRITE)
Worst xtor drop ~ 210mV

Xtor Level Voltage Drop of Mem2 (READ)
Worst xtor drop ~ 130mV

Mem1 Mem2
Two instantiations of same memory macro
Case Study: Touch Solution – Hierarchical Analog + Digital

Block level EMIR Analysis and Model Generation

Analog blocks (e.g.,) ADC, Clock gen, comparators

- Netlist (spice/spectre + dsdf)
- Layout / GDS
- TypicalTotem runtime <1hr

- Flatten design
- RC extraction
- CMM (electrical + physical db)

Digital blocks (e.g.,) Processor, SRAM, Flash, etc

- Design DEF
- Signal SDF/ STA File
- RTL/Gate Vcc/Isdb
- Typical Totem runtime <1hr

- Flatten design
- RC extraction
- Simulation
- CMM (electrical + physical db)

EM/IR Reports
GUI Maps

Totem enables full IP level Power Integrity sign-off w/o need for full IP level functional simulation decks

Full Top level EMIR Analysis

- Tech File
- Top level GDS
- User Constraints
- Pad locations
- Pkg Model

- Flatten design
- RC extraction
- DC/Transient Simulation

EM/IR Reports
GUI Maps

Typical Totem runtime< few hrs
Case Study: Touch Solution – ESD Concerns

- Higher Integration → Multiple power domains
- More PG domains → More ESD pathways
- Larger devices → Latch up immunity

Higher Integration  →  ESD and Latch Up immunity concerns
Reliability Checks

Focus: Mitigate Latch-up and ESD Risks

- Guard Ring Weakness
- Res checks (HBM/MM)
- Current-density checks
- System level ESD (IEC-61000-4-2)

Guard Ring Weakness Maps

Guard ring was connected through M1 to the grid
Hence violating the 20ohm Constraint
Reliability Checks

**Focus: Mitigate Latch up and ESD Risks**

- Guard Ring Weakness
- Res checks (HBM/MM)
- Current-density checks
- System level ESD (IEC-61000-4-2)

**Reliability**

- Latch-up/ESD

**Resistance Checks**

**Current Density Checks**

- Current Density ESD Failure
Totem: Power-Noise-Reliability Platform

<table>
<thead>
<tr>
<th>Early PG Planning For IP Design</th>
<th>Dynamic Sign off</th>
<th>Reliability Sign Off</th>
<th>Soc Integration</th>
</tr>
</thead>
<tbody>
<tr>
<td>Grid Weakness</td>
<td>DvD Analysis</td>
<td>Vectored/Vless EM</td>
<td>IP modeling for SoC</td>
</tr>
<tr>
<td>Missing Via Check</td>
<td>Substrate Noise</td>
<td>ESD Connectivity</td>
<td>SoC Power Integrity</td>
</tr>
<tr>
<td>Static IR</td>
<td>AMS support</td>
<td>ESD Current density</td>
<td>Chip Power Modeling</td>
</tr>
</tbody>
</table>

- Early design closure
- Increased coverage
- Mitigate failures
- IP hand-off

IP Sign-off Benefits with Totem
Thank you for your time and attention!